Notice of Allowability	Application No.	Applicant(s)	
	09/853,998	MATSUI, TSURUTO	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *9/13/04*.

2. ☒ The allowed claim(s) is/are *1-8*.

3. ☒ The drawings filed on *13 September 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☒ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Guy J. Lamarre
Primary Examiner

Drawings

The drawings were received on September 13, 2004. These drawings are acceptable.

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on May 19, 2000. It is noted, however, that applicant has not filed a certified copy of the 2000-152776 application as required by 35 U.S.C. 119(b).

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

The present invention pertains to a pattern generator and pattern generation method for a semiconductor test apparatus for freely generating inverse request signals for inverting the read/write data for specified memory cells in a memory device having different numbers of memory cells between X and Y directions. The claimed invention recites the features "...an inversion request signal circuit for generating an inversion request signal for each specified memory cell of a semiconductor memory device under test for inverting write data to the specified memory cell; wherein locations of specified memory cells are on a diagonal line on an array of memory cells in the semiconductor memory device under test, and wherein overall numbers of memory cells in a row (X) and column (Y) are different from each other..."

The prior arts of record (Lepejian et al. U.S. Patent No. 6,011,748 as an example of such prior arts) teach a method of independently controlling the row and column addressing of a semiconductor memory by a BIST circuit and also allows for use of different patterns of rows and columns during test to accommodate memories having address spaces of different sizes or configurations. However, the prior arts of record fail to teach "...an inversion request signal circuit for generating an inversion request signal for each specified memory cell of a semiconductor memory device under test for inverting write data to the specified memory cell; wherein locations of specified memory cells are on a diagonal line on an array of memory cells in the semiconductor memory device under test, and wherein overall numbers of memory cells in a row (X) and column (Y) are different from each other..." As such, modification of the prior arts of record can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior arts themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior arts of record to encompass the limitations set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the claimed inventions. Hence, claims 1-8 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

Guy J. Lamarre
Primary Examiner